REMARKS

Summary of the Office Action

Claims 1-3 and 5-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shigemoto (US 5,923,570) in view of Andresen et al. (US 6,147,538).

Applicant wishes to thank the Examiner for the indication that claims 10, 11, 15, and 16 contain allowable subject matter.

Summary of the Response to the Office Action

Applicant has amended claims 1 and 5 to further define the invention. Accordingly, claims 1-3, 5-11, 15, and 16 are pending for reconsideration.

All Claims Define Allowable Subject Matter

Claims 1-3 and 5-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shigemoto (US 5,923,570) in view of Andresen et al. (US 6,147,538). Applicant respectfully traverses the rejection as being based upon a combination of references that neither teaches nor suggests the novel combination of features recited in independent claims 1 and 5, and hence dependent claims 2, 3, 6-11, 15, and 16.

Independent claims 1 and 5, as amended, both recite a semiconductor integrated circuit device including "a plurality of external signal input/output circuits having input protection circuits connected to input/output terminals outside said internal circuits" and active elements "in a second connection configuration for protecting said active element in the first connection configuration arranged adjacent to said active element in the first connection configuration." At least these features of amended independent claims 1 and 5 are neither taught nor suggested by Shigemoto and Andresen et al., whether taken singly or combined.

The Office Action admits that Shigemoto does not disclose "the rest of the elements of the claim associated with an ESD protection circuit." Thus, the Office Action relies upon Andresen et al. for teaching an ESD protection circuit, as shown in FIGs. 3, 5, and 6, and alleges that the multi-finger transistors N2 and N1 are the "active element in a first connection configuration" and the "plurality of other active elements," of claims 1 and 5. As a result, the Office Action alleges that it would have been obvious to combine Shigemoto and Andresen et al. "because as Andersen et al. state (col. 1, line 11 – col. 2, line 15), the semiconductor IC's, especially modern MOS technology are highly vulnerable to the ESD events and must be protected from them." Applicant respectfully disagrees.

Neither of Shigemoto nor Andresen et al., whether taken singly or combined, teaches or suggests a semiconductor integrated circuit device including at least "a plurality of external signal input/output circuits having input protection circuits connected to input/output terminals outside said internal circuits" and active elements "in a second connection configuration for protecting said active element in the first connection configuration arranged adjacent to said active element in the first connection configuration," as recited by amended independent claims 1 and 5, and hence dependent claims 2, 3, 6-11, 15, and 16.

Initially, Applicant respectfully submits that Shigemoto is non-analogous art with respect to Applicant's claimed invention. MPEP § 2141.01(a) instructs that "[in] order to rely on a reference as a basis for rejection of an Applicant's invention, the reference must either be in the field of Applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the invention was concerned. *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992)." Accordingly, since Shigemoto is directed toward a clock wiring method

and Applicant's claimed invention is directed to input protection circuitry, Applicant respectfully asserts that Shigemoto is non-analogous art.

Moreover, MPEP § 2141.01(a) instructs that "[a] reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem; and *Wang Laboratories Inc. v. Toshiba Corp.*, 993 F.2d 858, 26 USPQ2d 1767 (Fed. Cir. 1993)." Accordingly, since Shigemoto provides for a novel clock wiring design method and Applicant's invention is directed toward a semiconductor integrated circuit device with enhanced resistance to electrostatic breakdown, Applicant respectfully further asserts that Shigemoto is non-analogous to Applicant's claimed invention.

Furthermore, MPEP § 2143.01 instructs that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)." Although Andresen et al. appears to teach the desirability to protect integrated circuits from damage resulting from high voltage electrostatic discharge events, Shigemoto teaches an unrelated clock wiring design method. Thus, the combined teachings of Shigemoto and Andresen et al. fail to make obvious the claimed invention of amended independent claims 1 and 5. For example, the generic flip-flop devices taught by Shigemoto are incomparable to the specific MOS transistor structures taught by Andresen et al. Accordingly, Applicant respectfully asserts that there is no suggestion in Shigemoto to provide for electrostatic discharge protection and further there is no suggestion in Andresen et al. to provide electrostatic discharge protection

to clock wiring circuitry. In addition, Applicant respectfully submits that Andresen et al. teaches a single input protection circuit formed in external signal input/output circuits.

Thus, Applicant respectfully asserts that Shigemoto nor Andersen et al., whether taken singly or combined, fail to teach or suggest a semiconductor integrated circuit device including at least "a plurality of external signal input/output circuits having input protection circuits connected to input/output terminals outside said internal circuits" and active elements "in a second connection configuration for protecting said active element in the first connection configuration arranged adjacent to said active element in the first connection configuration," and recited by amended independent claims 1 and 5, and hence dependent claims 2, 3, 6-11, 15, and 16.

For the above reasons, Applicant respectfully asserts that the rejection under 35 U.S.C. § 103(a) should be withdrawn because Shigemoto nor Andresen et al., whether taken individually or in combination, neither teaches nor suggests the novel combination of features recited in independent claims 1 and 5, and hence dependent claims 2, 3, 6-11, 15, and 16.

Conclusion

In view of the foregoing remarks, Applicant respectfully requests reconsideration and the timely allowance of the pending claims. Should the Examiner believe that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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